ABSTRACT OF THE DISCLOSURE

A phase detector in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain. The phase detector includes a series of flip flops disposed in parallel that sample the second clock signal with both a rising edge of the first clock signal and a falling edge of the first clock signal. By tracking movement in one-to-zero or zero-to-one transitions in the sampled clock signals, the phase detector is operable to determine the phase difference between the first and second clock signals.